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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,038	05/11/2001	Richard J. Grupp	BUR920000214US1	8170

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/854,038	GRUPP ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 have been presented for examination based on the application filed on 11 May 2001.

Claim Interpretation

2. Applicants are claiming a two-port two-path bidirectional wire model. As best understood by the examiner, the term "port" is interpreted as a "node" in the electrical net. Also "path" defined in the claim is understood as a "net" or "wire" which connects the two nodes directly or indirectly. Claims further describe a control mechanism that inhibits the change on first path if the change is happening on the second path. This control mechanism to the examiner is interpreted as a multiplexer or a logic gates that could enable or disable the appropriate nets.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-10, 11-16, 22-23, 25-33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-10 & 11-16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter, software per se. Claims 1 & 11 are not tangibly embodied so as to be executable by a computer. Claims 2-10 and 12-16 are rejected on basis their dependency upon claims 1 and 11 respectively.

Claims 22-23 & 25-33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In claim 22 "signal bearing media" is defined in the specification (Pg 9-Line7-9) to include tangible items ("recordable type media") and items which are non-tangible ("transmission type media"). Therefore the claim as whole is not directed towards a tangible medium. It is suggested "signal bearing media" be changed to "recordable media" to overcome this rejection. Claims 23 and 25-33 are rejected on basis their dependency upon claims 22.

Claim Rej cti ns - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 1-6,10-12, 15-18, 20, 22-29 & 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5,202,593 issued to Huang in view of US Patent 6,496,955 issued to Chandra.

Regarding Claim 1

Huang discloses in Fig.1, a first path (element 13) between first port (element 12) and second port (element 14). Further, Huang discloses in Fig.1, a second path (element 11) between second port (element 14) and first port (element 12). Huang also discloses a buffer, a three-input NOR-gate and a single-shot device (Col. 2-Line54-56). NOR gate and a single-shot device act as control mechanism (Col. 1-Line 20-22). The control mechanism senses the change between the ports (Fig.1-Element 12 & 14) and drives the second port with the same input signal as the first port (Col. 2-Line 28-37). The control mechanism also enable the appropriate path by disabling the second path until the driving signal is asserted on the first port (Col. 2-Line 38-47), hence only one path is driving the ports at any given time. The same reasoning works when the signal is asserted on the second port and it drives the first port.

Huang does not disclose that circuit is a *model for representing a bidirectional wire* [bus] *input/output (I/0) during computer simulation.*

Chandra teaches us that a module[1] can be represented in high-level HDLs such as Verilog hardware description language (HDL) or VHDL written in RTL or transistor level using primitives provided by HDL (Col. 4-Line 7-20). Verilog or

[1] A module can represent pieces of a hardware system ranging from simple logic gates to complete systems, e.g. a computer. In our case this module is a circuit.

VHDL module is a model of actual circuit that can be executed on a computer and Chandra teaches us how create such a module (Col. 4-Line 21-44, Line 60-67) by example.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to modify the teachings suggested by Huang and implement them in Verilog or VHDL as disclosed by Chandra. Chandra's teachings would allow users of Huang's circuit to perform circuit analysis on a bi-directional I/O wire in an expeditious manner through simulation. Issues like timing constraints can be addressed and captured at simulation time before fabrication of the actual circuit containing bidirectional I/O wires is done. Further motivation comes from Chandra as he teaches the need to perform functionality checks and other simulations of the models in view of growing complexity of digital systems (See: Chandra, Background).

Regarding Claims 2 & 3

Claims 2 & 3 are rejected as Chandra teaches that HDLs like Verilog or VHDL can be used to implement the model (Col. 4-Line 7-20).

Regarding Claim 4

Huang discloses 3-input-NOR gate (Fig.1 elements 24 & 26) and details of a buffer (Fig. 2). The buffer comprises of two NMOS, only one of them in the path at any given time.

Regarding the claims limitation that two NMOS devices are used in each path, Huang teaches that each path comprises a NOR gate and a buffer. These

devices inherently include at least one NMOS each as depicted in Fig.1 (Huang) and Fig.2 (Huang).

Regarding Claim 5

Huang discloses a quiescent state when no external buses (net) are driving the ports. The ports remain in high logic level (Col. 1-Line 36-40). When one of the external nets drives input net [port](Fig.1 element 12) low, the first unidirectional path (Fig.1 element 13) pulls the other net [port] low (Fig.1 element 14) (Col. 1-Line 40-42). A control signal is also issued to the disable the other unidirectional path (Fig.1 element 11) (Col. 1-Line 50-65). The 3-input-NOR (Fig.1 element 26) in the first path (Fig.1 element 13) feeds back on 3-input-NOR (Fig.1 element 24) in the second path (Fig.1 element 11) through input AU (& AD). This feedback input from first path enables (or disables) the second path. This input goes into an NMOS device, which is comprised in the 3-input-NOR gate (as mentioned in the conventional 3-input-NOR design in the preceding claim). Hence, Huang replicates the mechanism mentioned in the claim above.

Regarding Claim 6

Chandra Teaches Huang that circuits can be modeled using Verilog or VHDL. Hence the NMOS mentioned in claim 4 could be modeled using Verilog NMOS primitives when Verilog is used as HDL.

Regarding Claim 10

Huang discloses that the control mechanism disables the second path until the driving signal is asserted on the first port [and path] (Col. 1-Line 50-65), hence

only one path is driving the ports at any given time. Observing the Fig.1, this is true vice versa also.

Regarding Claim 11

Claim 11 recites the same limitations as claim 1. Additionally, it includes second NMOS in first path and first NMOS in second path. Claim 11 is rejected in the view of reasons mentioned in claim 1 & claim 4 rejections done above.

Regarding Claim 12

Claim 12 is dependent claim of claim 11 and it discloses the third NMOS and forth NMOS devices as pass devices. Claim 12 is rejected on accord of Huang in view of Chandra, who discloses a buffer (Fig. 2), which is a pass device comprising of NMOS devices.

Regarding Claim 15

Claim 15 is rejected for the same reasons as claim 6 mentioned above.

Regarding Claim 16

Claim 16 is rejected for the same reasons as claim 10 mentioned above.

Regarding Claim 17

Claim 17 is an independent claim and is rejected for the same reason as claim1 mentioned above.

Regarding Claim 18

Claim 18 is rejected for the same reasons as claim 10 mentioned above.

Regarding Claim 20

Claim 20 is rejected for the same reasons as claim 4 mentioned above.

Regarding Claim 22

Claim 22 part A recites same claim limitations as claim 1. 22-A is rejected for afore mentioned reasons for claim 1. Additionally, it includes a "signal bearing media" in part B of the claim.

Disclosure by Huang is mentioned before. Huang does not teach a about a signal bearing media bearing the hardware description language (HDL) model.

Chandra teaches that a model could be captured in a HDL [RTL description] and stored on a storage device, which communicates with a computer (Col. 5-Line 66-67, Col. 6-Line 1-3).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made that teaching of Chandra can be applied to Huang to store the model on a storage device [recordable media]. The motivation would be the ability to retrieve from storage device the model to simulate & test the behavior of bidirectional I/O wire.

Regarding Claims 23 & 24

Claim 23 & 24 are rejected in view of Chandra's teachings in the previous claim. Chandra also discloses a terminal being used (Col. 6-Line 12-15), which inherently includes the transmission media that will transport the result from the processor to the calling terminal.

Regarding Claims 25 & 26

Claim 25 & 26 are rejected for the same reasons as claim 2 & 3 mentioned above.

Regarding Claim 27

Claim 27 is rejected for the same reasons as claim 4 mentioned above.

Regarding Claim 28

Claim 28 is rejected for the same reasons as claim 5 mentioned above.

Regarding Claim 29

Claim 27 is rejected for the same reasons as claim 6 mentioned above.

Regarding Claim 33

Claim 33 is rejected for the same reasons as claim 10 mentioned above.

5. Claim 7-9,13-14,19, 21 & 30-32 ar rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5,202,593 issued to Huang in view of US Patent 6,496,955 issued to Chandra as applied to rejection of claims 1-6,10-12, 15-18, 20, 22-29 & 33 above, further in view of in view of US Patent 5,396,435 issued to Ginetti.

Regarding Claim 7

Huang in view of Chandra disclose a bidirectional I/O modeled in Verilog using NMOS gates as discussed above.

Huang and Chandra do not teach annotated timing values to include the input port delays from the NMOS.

Ginetti discloses that timing path delay values at an input port of a primitive cell is represented by a capacitance.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to take the teachings of Ginetti and apply them to Huang & Chandra's teachings. They would teach that in a Verilog model created by Huang & Chandra, delays in the primitive cells, like NMOS cells, could include input port delays. Hence timing values annotated in the model can include input port delays. The third NMOS would map to the NMOS in the buffer (Fig.1 element 18 instance of Fig2, element T1 & T2) and the forth NMOS would map to the NMOS in the buffers as well (Fig.1 element 16 instance of Fig2, element T1 & T2). The motivation to annotate the values in the timing of the any NMOS cell would be to get more realistic timing delay across the bidirectional wire I/O model/method.

Regarding Claim 8

An analysis of Fig.1 (Huang) reveals that Huang & Chandra teaches the claimed controlled circuit wherein it can be seen from Fig. 1 that unidirectional paths (elements 11 & 13) comprise of control circuit (element 20, 26, 24 & 22) and output buffers (16 & 18), which can be modeled into Verilog or VHDL primitives & gates.

Huang & Chandra do not disclose annotating the timing on the two unidirectional paths that he discloses.

Ginetti discloses that timing path between input and output of each primitive cell is approximated by gate propagation delay (Col. 2-Line 35-43).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to modify the teachings suggested by Ginetti and apply them to Huang & Chandra, by breaking up each path into individual subcomponents and primitive cells and then adding up the gate propagation delay information to annotate the timing values across the first path and second path. Hence, Ginetti's teachings would allow user of the Huang & Chandra's system to more accurately calculate the delays between the two unidirectional paths. Further, Ginetti teaches that any circuit can be modeled into a Verilog or VHDL (Col. 1-Line 59-64).

Regarding Claim 9

Delays are calculated between the first port and second port and vice versa. Ginetti also discloses that the timing delays further include load dependent delays and port capacitances (Col. 2-Line 40-42). Ginetti goes on to give all the delay components to annotate the timing information (Col. 2-Line 43-55) between the input and the output ports of a primitive cell (e.g. primitive NMOS device)

Regarding Claim 13

Claim 13 is rejected for the same reasons as claim 7 mentioned above.

Regarding Claim 14

Claim 14 is rejected for the same reasons as claim 9 mentioned above.

Regarding Claim 19

Claim 19 is rejected for the same reasons as claim 8 mentioned above.

Regarding Claim 21

Claim 21 is rejected for the same reasons as claim 7 mentioned above.

Regarding Claim 30

Claim 30 is rejected for the same reasons as claim 7 mentioned above.

Regarding Claim 31

Claim 31 is rejected for the same reasons as claim 8 mentioned above.

Regarding Claim 32

Claim 32 is rejected for the same reasons as claim 9 mentioned above.

End of claim rejections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
Examiner
Art Unit 2128

as

JEAN HOMERE
SUPERVISORY PATENT EXAMINER